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Jason Gosior

9171

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7590

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EXAMINER

LI, AIMEE J

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/843,178

Applicant(s)

GOSIOR ET AL.

Examiner

Aimee J. Li

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☒ Claim(s) 1 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-20 have been considered. Claim 1 has been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 14 March 2006 and Extension of Time for 3 Months as received on 14 March 2006.

Claim Objections

3. Claim 1 is objected to because of the following informalities: Please correct line 7 from - "k'-- to read -[["']k'--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM).
6. Regarding claim 1, Li has taught a programmable, single-chip embedded processor, comprising:

- a. A multiple-bit, multithread processor core comprising a single processor pipeline having 'k' pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and the number 'n' of said processor threads being equal to or less than 'k' (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3);
- b. An instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3);
- c. A supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3);

- d. A memory capable of storing data comprising instructions from said instruction set (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3); and
- e. Wherein:
 - i. Each or the 'n' program threads occupies a unique pipeline stage at any given time (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3);
 - ii. Each program thread advances to the next pipeline stage with every clock cycle (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3); and
 - iii. For a given program thread, the pipeline completes a one-word instruction every 'k' clock cycles (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation,

paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3).

7. Li has not taught
 - a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;
 - b. Said memory being internally integral to the processor, and comprising a main RAM and a boot ROM; and
 - c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core.
8. ARM has taught
 - a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation (ARM page 291);
 - b. Said memory being internally integral to the processor (ARM page 271), and comprising a main RAM and a boot ROM (ARM pages 20 and 271); and
 - c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core (ARM pages 216-217).
9. A person of ordinary skill in the art at the time the invention was made, and as taught by ARM, would have recognized that the details of an embedded system such as ARM reduces

Art Unit: 2183

power consumption by minimizing off-chip activity, e.g. fewer loads from off-chip memory, and increases parallelism (ARM pages 31-32). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the embedded details of ARM in the device of Li to reduce power consumption.

10. Regarding claim 3, Parady has taught a system as recited in claim 1, wherein said processor core supports "n" multiple groups of independent threads by replicating said common execution logic and said memory (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3).

11. Claims 2, 6-7, 9-10, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady).

12. Li has taught wherein said memory comprises internal memory for storing and executing core processor code (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). Li has not taught

- a. (Claim 2) A system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage, instruction decode logic stage, multiple port

register read stage, address mode logic stage, arithmetic logic unit for arithmetic and address calculations stage, multiple port memory stage, branch/wait logic stage, and multiple port register write stage;

- b. (Claim 6) A system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity;
 - c. (Claim 7) A system as recited in claim 1, wherein said supervisory control unit is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation;
 - d. (Claim 9) A system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions;
 - e. (Claim 10) A system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads;
 - f. (Claim 16) A system as recited in claim 1, wherein said memory comprises external memory engaged with said peripheral adaptor; and
 - g. (Claim 17) A system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.
13. Parady has taught
- a. (Claim 2) A system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage (Parady Col.3 lines 2-9), instruction decode logic

stage (Parady 14 of Fig.3), multiple port register read stage (Parady 48/50 of Fig.3), address mode logic stage (Parady Col.3 lines 2-9), arithmetic logic unit for arithmetic and address calculations stage (Parady Col.3 lines 50-56), multiple port memory stage (Parady 48/50 of Fig.3), branch/wait logic stage (Parady 18 of Fig. 1), and multiple port register write stage (Parady 48/50 of Fig.3). Here, the functions are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Col.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion.

- b. (Claim 6) A system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity (Parady Fig.4 and Col.3 line 66 - Col.4line 8). Here, certain instructions can enable a specific thread upon a thread switch, thus determining the identity of the thread that is desired to be switched to.
- c. (Claim 7) A system as recited in claim 1, wherein said supervisory control unit (Parady 112 of Fig.3) is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation (Parady Col.3 lines 57-65). Here, the thread switching logic monitors the processing core for a cache miss, and if it determines there was a cache miss, can stop the current thread and start a new thread (Parady Col.3 lines 57-65), as well as put the threads into interleaving mode (Parady Col.4 lines 18-29).

- d. (Claim 9) A system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions (Parady Col.3 line 57 - Col.4 line 8). Here, each thread can access the thread switching logic by providing it with a thread ID to switch to upon a long-latency operation which is detected by the thread switching logic, the thread ID which can be provided in a load or store (input/output) instruction (see Col 4 lines 5-7).
- e. (Claim 10) A system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads (Parady Col.3 line 57 – Col 4 line 8). Here, any of the four threads can cause a cache miss to be detected by the thread switching logic (Parady Col.3 lines 57-65), and can further be programmed to include a thread field that tells the thread switching logic which thread to switch to (Parady Col 4 lines 1-8).
- f. (Claim 16) A system as recited in claim 1, wherein said memory comprises external memory engaged with said peripheral adaptor (Parady 176/180 of Fig.5).
- g. (Claim 17) A system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core (Parady Fig.3). Here, the thread switching logic is separate from the core functions of fetch, decode, issue and execute.

14. A person of ordinary skill in the art at the time the invention was made, and as taught by Parady, would have recognized that the device of Parady improves thread switching efficiency (Parady Col. 2 lines 15-16). Therefore, it would have been obvious to a person of ordinary skill

Art Unit: 2183

in the art at the time the invention was made to incorporate the device of Parady in the device of Li in view of ARM to improve thread switching efficiency.

15. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Dickman et al., U.S. Patent No. 4,556,951 (herein referred to as Dickman).

16. Regarding claim 4, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises a condition code mechanism implemented in said instruction set for detecting specific word data types. However, Dickman has taught a system for detecting specific word data type and setting corresponding condition codes so that conventional program control instructions can be used to control processing, rather than modifying existing control instructions to do so (Dickman Col.2 line 57 - Col.3 line 5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to detect specific types of data words and set their corresponding condition codes so that existing control instructions can be used, thereby creating less work and preserving the previous compatibility of the instruction set.

17. Regarding claim 5, Li in view of ARM and in further view of Dickman has taught a system as recited in claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range (Dickman Col.8 line 63 - Col.9 line 12).

18. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE

Art Unit: 2183

©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady), as applied to claim 7 above, and further in view of Miyamoto et al., U.S. Patent No. 6,101,569 (herein referred to as Miyamoto).

19. Regarding claim 8, Li in view of ARM and in further view of Parady has taught a system of claim 7, but has not explicitly taught wherein the system further comprises a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral and system memory. However, Miyamoto has taught a semaphore vector (Miyamoto Cots lines 34-51) which controls multithread access to peripherals and system memory (Miyamoto Col.4 line 66 - Col.5 line 33) so that data is not inadvertently destroyed by another thread (see Col.1 lines 21-36). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to include the use of hardware semaphore vector to control access to peripherals and memory so that inadvertent data destruction does not take place, and thus incorrect operation does not result.

20. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady), as applied to claim 9 above, and further in view of Fernando et al., U.S. Patent No. 6,272,616 (herein referred to as Fernando).

21. Regarding claim 11, Li in view of ARM and in further view of Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating core processor thread is capable of reconfiguring the overall thread processing method of operation so that other processing threads can support multiple instruction multiple data processing operations. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (Fernando Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for an instruction that lets the processing threads switch into MIMD mode in order to improve processing performance for a broad range of software types.

22. Regarding claim 12, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread can reconfigure the overall thread processing method of operation so that other processing threads can support single instruction multiple data processing operations. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (Fernando Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for an instruction that lets the processing threads switch into SIMD mode in order to improve processing performance for a broad range of software types.

Art Unit: 2183

23. Regarding claim 13, Li in view of ARM and in further view of Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread is capable of reconfiguring the overall thread processing method of operation so that an arbitrary number of processing threads can support simultaneously single instruction multiple data processing operations and multiple instruction multiple data processing operations. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Co1.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (Fernando Col.2 lines 27-32), which allows SIMD and MIMD modes to be concurrently executing (Fernando Col.12 lines 1-5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for the processing threads to simultaneously execute in both SIMD mode and MIMD mode in order to improve processing performance for a broad range of software types.

24. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Bishop et al., U.S. Patent No.5, 784,552 (herein referred to as Bishop).

25. Regarding claim 14, Li in view of ARM has taught the system as recited in claim 1, but has not explicitly taught wherein said supervisory control unit is operable by a first thread process to start and stop another thread process and to examine and alter state information in single step and multiple step modes of controlled operation. However, Bishop has taught the

Art Unit: 2183

execution of an application program under the supervision of a debugging program, the debugging program which halts the application program (Bishop Col.5 lines 11-22) and can examine and alter state information via debugging instruction execution in either single-step or multi-step modes of debugging (Bishop Col.7 lines 13-45) so that an application programmer can more thoroughly test and debug their programs in a controlled testing environment (Bishop Col.1 lines 17-35). One of ordinary skill in the art would have recognized that thoroughly tested and debugged programs are less likely to fail and provide incorrect results. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to allow a debugging program to stop and start another program so that instructions in the other program can be thoroughly tested and debugged in both single-step and multi-step modes of debugging.

26. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Zammit et al., European Patent Application No. 1091292 (herein referred to as Zammit).

27. Regarding claims 15 and 19-20, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught

- a. Wherein the system further comprises identifying bit patterns embedded in the unassigned bit fields of the machine instructions of said core processor (Applicant's claim 15);

- b. Wherein said identifying bit pattern is used to identify programming code for code protection purposes (Applicant's claim 19); and
- c. Wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism (Applicant's claim 20).

28. However, Zammit has taught a processor which identifies values in unused bit fields of instruction during a conversion so that the unused bit fields which contain inappropriate values, which could result in incorrect translation, can be corrected before being executed (see p3 lines 9-16, 35-39). This bit pattern also protects programming code from being incorrectly translated and causing incorrect execution of the program code. This bit pattern also does not affect the instruction execution logic operation, since it is only used to identify whether there are unused bit fields, which contain in appropriate values, and does not cause the execution logic to perform differently from what the instruction intended. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of Arm to identify values of unused bits so that inappropriate values are not incorrectly translated, and thus incorrect execution does not occur.

29. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Wilske, U.S. Patent No. 4,155,115 (herein referred to as Wilske).

30. Regarding claim 18, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught wherein said peripheral adaptor is capable of controlling analog and digital

Art Unit: 2183

processing functions. However, Wilske has taught a microprocessor system which has a peripheral controller capable of receiving and controlling inputs from both analog and digital sources (Wilske Col.2 lines 7-34) so that both types of sources can be controlled from one location in order to reduce cost and lessen hardware (Wilske Col.1lines 14-24). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to allow its peripheral adapter to control both analog and digital sources so that the amount of hardware needed to control both types of sources can be reduced, thus lowering cost.

Response to Arguments

31. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

- a. Dirceu Cavendish's "CORPS – A Pipelined Fair Packet Scheduler for High Speed Switches" IEEE ©2000 has taught switching with round-robin scheduling.

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

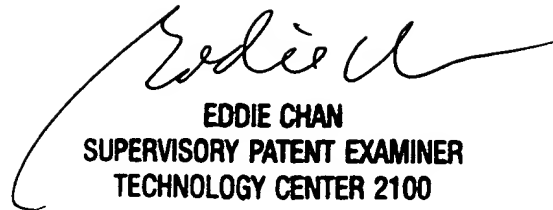
37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 09/843,178

Page 18

Art Unit: 2183

Aimee J. Li
27 April 2006



EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100